

558145

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property
Organization
International Bureau



(43) International Publication Date
9 December 2004 (09.12.2004)

PCT

(10) International Publication Number
WO 2004/107190 A1

(51) International Patent Classification⁷: G06F 13/40

(21) International Application Number:
PCT/IB2004/050718

(22) International Filing Date: 17 May 2004 (17.05.2004)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
03101537.3 27 May 2003 (27.05.2003) EP

(71) Applicant (for all designated States except US): KONINKLIJKE PHILIPS ELECTRONICS N.V. [NL/NL]; Groenewoudseweg 1, NL-5621 BA Eindhoven (NL).

(72) Inventors; and

(75) Inventors/Applicants (for US only): KATOCH, Atul [IN/NL]; c/o Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL). GARG, Manish [IN/NL]; c/o Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL). SEEVINCK, Evert

[NL/NL]; c/o Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL). VEENDRICK, Hendricus, J., M. [NL/NL]; c/o Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).

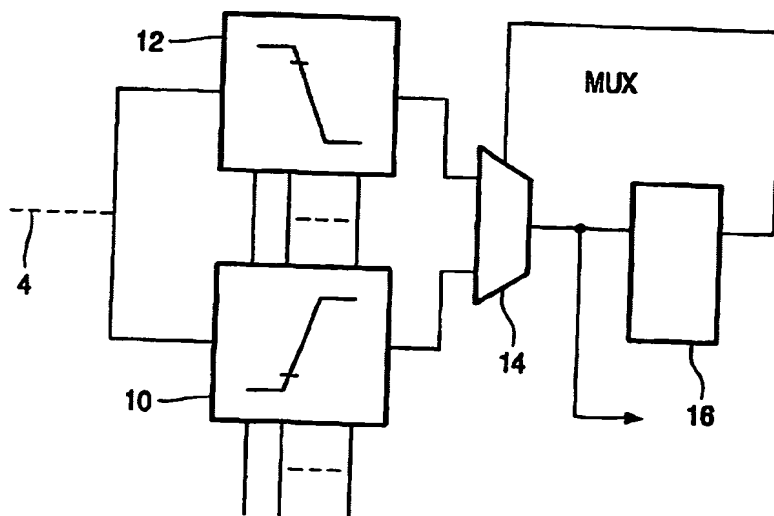
(74) Agent: ELEVELD, Koop, J.; Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PL, PT, RO, SE, SI,

[Continued on next page]

(54) Title: OPERATING LONG ON-CHIP BUSES



(57) Abstract: As technology scales, on-chip interconnects are becoming narrower, and the height of such interconnects is not scaling linearly with the width. This leads to an increase of coupling capacitance with neighboring wires, leading to higher crosstalk. It also leads to poor performance due to poor RC response at the receiving of the wire, which may even result in failure in very noisy environments. An adaptive threshold scheme is proposed in which receiver switching thresholds are adjusted according to the detected noise in bus lines. These noise levels are dependent on both the front-end processing (transistor performance) as well as on the backend processing (metal resistance, capacitance, width and spacing). The circuit therefore automatically compensates for process variations.

~~This Page Marked (copy)~~
BEST AVAILABLE COPY

WO 2004/107190 A1